ABSTRACT OF THE DISCLOSURE

A circuit for reducing power in an on-chip cache memory on a microprocessor chip is implemented by dynamically controlling power applied to individual memory sections. Individual sections of memory are isolated from a fixed power supply by inserting one or more switches between GND and a negative connection of an individual memory section or by inserting one or more switches between VDD and a positive connection of an individual memory section. If a memory section is not accessed for a defined time, a PMU (Performance Monitor Unit) detects it and the power to that section is switched off, saving power. In addition, a software application may send information to the PMU to select the amount of cache memory needed for the particular software application.